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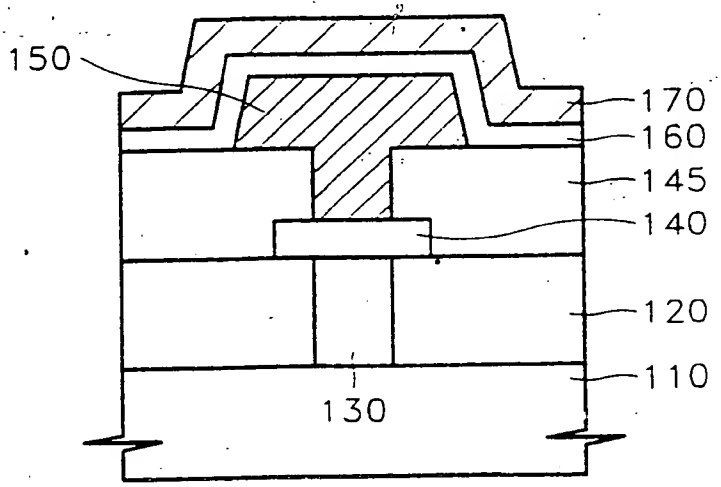
(54) A method for manufacturing a capacitor for a semiconductor device

(57) In a method for manufacturing a capacitor for a semiconductor device, a first interlayer insulating layer (120) is formed to have a first contact hole on a semiconductor substrate (110), and a contact plug (130) is formed to fill the first contact hole. A diffusion barrier layer pattern (140) is formed on the contact plug (130). A second interlayer insulating layer pattern (145) is formed to have a second contact hole which exposes the diffusion barrier layer pattern (140) on the resultant including the diffusion barrier layer pattern. A conductive layer pattern (150) is formed to make contact with the diffusion barrier layer pattern (140) through the second contact hole to complete a lower electrode including the contact plug, the diffusion barrier layer pattern (140), and the conductive layer pattern (150). Then, a dielectric layer (160) and an upper electrode are sequentially formed on the conductive layer pattern (150). In this manner, reduction of the capacitance of the capacitor can be prevented by preventing oxidation of the diffusion barrier layer pattern (140).

FIG. 6



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Description

The present invention relates to a method for manufacturing a capacitor for a semiconductor device, and more particularly, to a method for manufacturing a lower electrode of a capacitor to which a thin film having a high dielectric constant is applied.

The decrease of cell capacitance along with a decrease in the area of a memory cell places a serious obstacle in increasing the integration level of DRAMs. The decrease of cell capacitance impedes the operation of a device at a low voltage as well as lowering the reading ability of a memory cell and increasing the soft error rate.

The charge amount Q of a capacitor is the product of capacitor capacitance C and an operation voltage V. That is, $Q = C \times V$. Thus, to obtain a predetermined amount of charge with a decreased operation voltage, the capacitance should be increased. Assuming that the effective area of a capacitor is A, a dielectric constant in vacuum is ε_0, the relative dielectric constant of a dielectric ε_r, and the thickness of the dielectric is d, the capacitance C is given as $A\varepsilon_0\varepsilon_r/d$. Therefore, the capacitor capacitance C increases with a larger effective area A, a larger effective constant ε_r of a dielectric layer, and a smaller thickness d of the dielectric layer.

To increase the effective area of a capacitor, three-dimensional lower electrode structures such as fin, box, and cylindrical structures have been suggested. However, it is hard to apply these three-dimensional lower electrode structures in real situations since their manufacturing processes are complicated and defects are likely to occur during the manufacturing processes.

Accordingly, research has been actively conducted on making a thin film of a material of a high dielectric constant to increase the capacitance. A capacitor having the thin film of high dielectric constant is more preferred in terms of the high integration level of semiconductor devices as well as process simplication, because a capacitor to which a thin film having a high dielectric constant is applied can secure a sufficient capacitance with a simple two-dimensional lower electrode.

However, when a lower electrode is formed of impurity-doped polysilicon as in prior art, a material of a high dielectric constant reacts with polysilicon, and thus a new dielectric layer having a very low dielectric constant is formed at their interface, thereby decreasing the entire capacitance. Therefore, there is an increasing need for a new structure of a lower electrode suitable for a capacitor to which a thin film of a high dielectric constant is applied in a semiconductor device.

FIGS. 1, 2, and 3 are sectional views for explaining a conventional method for manufacturing a capacitor for a semiconductor device.

FIG. 1 illustrates the step of forming an interlayer insulating layer pattern 20 and a contact plug 30. The interlayer insulating layer pattern 20 is formed on a semiconductor substrate 10 to have a contact hole exposing a predetermined area of the semiconductor substrate 10. Subsequently, an impurity-doped polysilicon layer is formed on the resultant structure having the interlayer insulating layer pattern 20, to fill the contact hole. Then, the contact plug 30 is formed in the contact hole by completing etching the polysilicon layer till the interlayer insulating layer pattern 20 is exposed.

FIG. 2 illustrates the step of completing a lower electrode constituted of the contact plug 30, a diffusion barrier layer pattern 40, and a conductive layer pattern 50 by forming the diffusion barrier layer 40 and the conductive layer pattern 50. First, a diffusion barrier layer and a conductive layer are sequentially formed of a titanium nitride (TiN) and platinum (Pt), respectively, on the resultant structure having the contact plug 30 formed therein.

Then, the diffusion barrier layer pattern 40 and the conductive layer pattern 50 are formed to be sequentially stacked on the contact plug 30 by sequentially etching the conductive layer and the diffusion barrier layer till the interlayer insulating layer pattern 20 is exposed. that is, the lower electrode is completed. which has the contact plug 30, the diffusion barrier layer pattern 40, and the conductive layer pattern 50. The diffusion barrier layer pattern 40 serves to prevent the capacitance of a capacitor from decreasing due to reaction between the contact plug 30 and the conductive layer pattern 50 in a subsequent dielectric forming process.

FIG. 3 illustrates the step of completing the capacitor by forming a dielectric layer 60 and an upper electrode 70. First, an amorphous dielectric layer containing Ba, Sr, Ti, and O is formed on the resultant having the lower electrode formed thereon by chemical vapor deposition (CVD) or sputtering. Then, the resultant including the amorphous dielectric layer is heat-treated at 500-750°C so that the amorphous dielectric layer is crystallized. Thus, a crystalline dielectric layer 60 is formed of (Ba, Sr)TiO_2 of a perovskite structure. The crystalline dielectric layer 60 is referred to as the dielectric layer 60, hereinafter.

Alternatively, the dielectric layer 60 can be formed in an in-situ method where materials respectively containing Ba, Sr, Ti, and O are deposited on the resultant including the lower electrode, while the resultant including the lower electrode is being heat-treated at 500-750°C. Then, the upper electrode 70 is formed on the dielectric layer 60, thus completing the capacitor.

Anyway, the dielectric forming step is necessarily accompanied by the above-described heat treatment. Since a sidewall A of the diffusion barrier layer pattern 40 makes contact with the amorphous dielectric layer containing oxygen, the oxygen penetrates into the sidewall A of the diffusion barrier layer pattern 40 during the heat treatment, thus oxidizing the diffusion barrier layer pattern 40 and the contact plug 30. That is, materials having a low dielectric constants such as TiO_2 and SiO_2 are formed.

When the dielectric layer 60 is formed in in-situ, the

diffusion barrier layer pattern 40 and the contact plug 30 are also oxidized because the sidewall of the diffusion barrier layer pattern 40 is exposed to an oxygen atmosphere. In addition, the diffusion barrier layer pattern 40 and the contact plug 30 are likely to be oxidized by oxygen penetrating into the diffusion barrier layer pattern 40 through the conductive layer pattern 40.

Consequently, according to the conventional method for manufacturing a capacitor for a semiconductor device, though the diffusion barrier layer pattern 40 prevents the contact plug 30 and the conductive layer pattern 50 from reacting at their interface, oxygen penetrating into the sidewall of the diffusion barrier layer pattern 40 and the conductive layer pattern 50 during the step of forming the dielectric layer 60 oxidizes the diffusion barrier layer pattern 40 and the contact plug 30, thus producing materials of low dielectric constants such as TiO_2 and SiO_2. As a result, the capacitance of the capacitor is remarkably reduced.

According to a first aspect of the present invention, a method of manufacturing a capacitor for a semiconductor device, comprises the steps of:

(a) forming a first interlayer insulating layer having a first contact hole on a semiconductor substrate;
(b) forming a contact plug to fill said first contact hole;
(c) forming a diffusion barrier layer pattern on said contact plug;
(d) forming a second interlayer insulating layer pattern having a second contact hole which exposes said diffusion barrier layer pattern on the resultant including the diffusion barrier layer pattern;
(e) forming a conductive layer pattern to make contact with said diffusion barrier layer pattern through said second contact hole to complete a lower electrode including said contact plug, said diffusion barrier layer pattern, and a conductive layer pattern; and
(f) sequentially forming a dielectric layer and an upper electrode on said conductive layer pattern.

The contact plug may be formed of one selected from a group consisting of impurity-doped polysilicon, tungsten (W), tungsten nitride (WN), and tungsten silicide (Wsix), and the diffusion barrier layer pattern formed of one selected from a group consisting of Ta, Co, TiN, (Ti, Al)N, (Ti, Si)N, TaN, (Ta, Si)N, TiSix, TaSix, and CoSiX.

The conductive layer pattern may be formed of one selected from a group consisting of platinum (Pt), iridium (Ir), ruthenium (Ru), iridium dioxide (IrO_2), and ruthenium dioxide (RuO_2), and the contact plug, the diffusion barrier layer pattern, and the conductive layer pattern formed of impurity-doped polysilicon, titanium nitride (TiN), and platinum (Pt), respectively.

According to a second aspect of the present invention, a method of manufacturing a capacitor for a semiconductor device, comprises the steps of:

(a) forming a first interlayer insulating layer pattern having a first contact hole on a semiconductor substrate;
(b) forming a contact plug to fill the first contact hole;
(c) forming a first diffusion barrier layer pattern on the contact plug;
(d) forming a second interlayer insulating layer pattern having a second contact hole which exposes the first diffusion barrier layer pattern on the resultant including said first diffusion barrier layer pattern;
(e) forming a second diffusion barrier layer pattern to rill the second contact hole;
(f) forming a conductive layer pattern on the second diffusion barrier layer pattern to complete a lower electrode including the contact plug, said first diffusion barrier layer pattern, said second diffusion barrier layer pattern, and the conductive layer pattern; and
(g) sequentially forming a dielectric layer and an upper electrode on the conductive layer pattern.

The contact plug may be formed of one selected from a group consisting of impurity-doped polysilicon, tungsten (W), tungsten nitride (WN) , and tungsten silicide (Wsix), and the first diffusion barrier layer pattern formed of one selected from a group consisting of Ta. Co, TiN, (Ti, Al)N, (Ti, Si)N, TaN, (Ta, Si)N, TiSix, TaSix, and CoSix.

The second diffusion barrier layer pattern may be formed of one selected from a group consisting of Ir, Ru, IrO_2, and RUO_2, and the conductive layer pattern formed of Pt.

The second diffusion barrier layer may be formed to have a double-layer structure where Ir and IrO2 are sequentially stacted, and the conductive layer pattern is formed of Pt.

The method of manufacturing a capacitor for a semiconductor device according to the present invention prevents reduction of the capacitance of the capacitor due to oxidation of a portion of the lower electrode by preventing oxidation of the diffusion barrier layer pattern.

Examples of the present invention will now be described in detail with reference to the accompanying drawings, in which:

The above object and advantages will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

FIGS. 1, 2, and 3 are sectional views for explaining a conventional method for manufacturing a capacitor for a semiconductor device;
FIGS. 4, 5, and 6 are sectional views for explaining a method for manufacturing a capacitor for a semiconductor device according to an embodiment of

the present invention; and

FIGS. 7, 8, and 9 are sectional views for explaining a method for manufacturing a capacitor for a semiconductor device according to another embodiment of the present invention.

FIG. 4 illustrates the step of forming a first interlayer insulating layer pattern 120, a contact plug 130, and a diffusion barrier layer pattern 140. The first interlayer insulating layer pattern 120 is formed on a semiconductor substrate 110 to have a first contact hole exposing a predetermined area of the semiconductor substrate 110.

Then, a first conductive layer is formed on the resultant including the first interlayer insulating layer pattern 120, to fill the first contact hole. The first conductive layer is formed of impurity-doped polysilicon, tungsten (W), tungsten nitride (WN), or tungsten silicide (WSix). Subsequently, the contact plug 130 is formed in the first contact hole by completly etching the first conductive layer till the first interlayer insulating layer pattern 120 is exposed.

A diffusion barrier layer is formed of Ta, Co, TiN, (Ti, Al)N, (Ti, Si)N, TaN, (Ta, Si)N, TiSix, TaSix, or CoSix on the resultant including the contact plug 130. Here, the diffusion barrier layer serves to prevent reaction between the contact plug 130 and a conductive layer pattern 150 of FIG. 5. Then, the diffusion barrier layer pattern 140 is formed on the contact plug 130 by etching the diffusion barrier layer till the first interlayer insulating layer pattern 120 is exposed.

FIG. 5 illustrates the step of forming a second interlayer insulating layer pattern 145 and a conductive layer pattern 150, thus completing a lower electrode having the contact plug 130, the diffusion barrier layer pattern 140, and the conductive layer pattern 150.

First, a second interlayer insulating layer is formed on the resultant including the diffusion barrier layer pattern 140. Then, the second interlayer insulating layer pattern 145 is formed to have a second contact hole by etching the second interlayer insulating layer till the diffusion barrier layer pattern 140 is exposed. A second conductive layer is formed of platinum (Pt), iridium (Ir), ruthenium(Ru), iridium dioxide (IrO_2), or ruthenium dioxide (RuO_2).

Then, the conductive layer pattern 150 is formed on the second interlayer insulating layer pattern 145 to make contact with the diffusion barrier layer pattern 140 through the second contact hole by patterning the second conductive layer till the second interlayer insulating layer pattern 145 is exposed. That is, the lower electrode having the contact plug 130, the diffusion barrier layer pattern 140, and the conductive layer pattern 150 is completed.

FIG. 6 illustrates the step of completing the capacitor of the present invention by forming a dielectric layer 160 and an upper electrode 170. First, an amorphous dielectric layer is formed on the resultant having the completed lower electrode thereon. Then, the resultant is heat-treated to crystallize the amorphous dielectric layer, thus forming a crystalline dielectric layer 160 of $SrTiO_3$, $(BaSr)TiO_3$, $(Pb, Zr)TiO_3$, or $(Pb, Zr)(Ti, La)TiO_3$. Alternately, the crystalline dielectric layer 160 may be formed in in-situ, while the resultant including the lower electrode is heat-treated. The crystalline dielectric layer 160 is referred to as the dielectric layer 160, hereinafter. Then, the upper electrode 170 is formed on the dielectric layer 160, thus completing the capacitor of the present invention.

Here, since the diffusion barrier layer pattern 140 does not contact with the amorphous dielectric layer, oxygen cannot react with the diffusion barrier layer pattern 140 during the heat treatment, in contrast to the prior art. Therefore, oxidation of the diffusion barrier layer pattern 140 and the contact plug 130 is prevented. When the dielectric layer 160 is formed in in-situ, oxidation of the diffusion barrier layer pattern 142 and the contact plug 130 can be also prevented because the diffusion barrier layer pattern 142 is not exposed to an oxygen atmosphere.

Even if the second interlayer insulating layer 145 is thin based on its surface, it takes a larger amount time for oxygen to reach the diffusion barrier layer pattern 140 through the conductive layer pattern 150 because the conductive layer pattern 150 contacts the diffusion barrier layer pattern 140 through the second contact hole. Accordingly, oxidation of the diffusion barrier layer pattern 140 due to oxygen introduced through the conductive layer pattern 150 can be prevented.

FIGS. 7, 8, and 9 are sectional views for explaining a method for manufacturing a capacitor for a semiconductor device according to a second embodiment of the present invention.

FIG. 7 illustrates the step of forming a first interlayer insulating layer pattern 220, a contact plug 230, and a first diffusion barrier layer pattern 140. First, the first interlayer insulating layer pattern 220 is formed on a semiconductor substrate 210 to have a first contact hole exposing a predetermined area of the semiconductor substrate 210. Then, a first conductive layer is formed of impurity-dope polysilicon, tungsten (W), tungsten nitride (WN), or tungsten silicide (Wsix) to fill the first contact hole, on the resultant including the first interlayer insulating layer pattern 220. Subsequently, the contact plug 230 is formed in the first contact hole by completly etching the first conductive layer till the first interlayer insulating layer pattern 220 is exposed.

A first diffusion barrier layer is formed of Ta, Co, TiN, (Ti, Al)N, (Ti, Si)N, TaN, (Ta, Si)N, TiSix, TaSix, or CoSix on the resultant including the contact plug 230. Here, the first diffusion barrier layer serves to prevent reaction between the contact plug 230 and a second diffusion barrier layer pattern 247 of FIG. 8. Then, the first diffusion barrier layer pattern 240 is formed on the contact plug 230 by etching the first diffusion barrier layer till the interlayer insulating layer pattern 245 is exposed.

FIG. 8 illustrates the step of forming a second inter-

layer insulating layer 245 and a second diffusion barrier layer pattern 247.

First, a second interlayer insulating layer is formed on the resultant including the first diffusion barrier layer pattern 240. Then, the second interlayer insulating layer pattern 245 is formed to have a second contact hole by patterning the second interlayer insulating layer till the first diffusion barrier layer pattern 240 is exposed.

Then, a diffusion barrier layer is formed of iridium (Ir), ruthenium (Ru), iridium dioxide (IrO_2), or ruthenium dioxide (RuO_2) to fill the second contact hole, on the second interlayer insulating layer pattern 245. Here, the second diffusion barrier layer can be formed to have a double-layer structure where iridium and iridium dioxide are sequentially stacked to increase the adhesiveness between the second diffusion barrier layer and a conductive layer pattern 250 of FIG 9.

Then, the second diffusion barrier layer pattern 247 is formed in the second contact hole by completly etching the second diffusion barrier layer till the second interlayer insulating layer pattern 245 is exposed. Here, the second diffusion barrier layer pattern 247 serves to prevent oxidation of the first diffusion barrier layer pattern 240.

FIG. 9 illustrates the steps of completing a lower electrode including the contact plug 230, the first diffusion barrier layer pattern 240, the second diffusion barrier layer pattern 247, and the conductive layer pattern 250, and completing the capacitor of the present invention by forming a dielectric layer 260 and an upper electrode 270.

First, a second conductive layer is formed on the resultant including the second diffusion barrier layer pattern 247 using platinum (Pt). Then, the conductive layer pattern 250 is formed on the second diffusion barrier layer pattern 247 by patterning the second conductive layer till the second interlayer insulating layer pattern 245 is exposed. That is, the lower electrode having the contact plug 230, the first diffusion barrier layer pattern 240, the second diffusion barrier layer pattern 247, and the conductive layer pattern 250 is completed.

Subsequently, an amorphous dielectric layer is formed on the resultant having the completed lower electrode thereon. Then, the resultant including the amorphous dielectric layer is heat-treated to crystallize the amorphous dielectric layer, thus forming a crystalline dielectric layer 260 of $SrTiO_3$, $(BaSr)TiO_3$, $(Pb, Zr)TiO_3$, or $(Pb, Zr)(Ti, La)TiO_3$. Alternativly, the crystalline dielectric layer 160 may be formed in in-situ, while the resultant including the lower electrode is heat-treated. The crystalline dielectric layer 260 is referred to as the dielectric layer 260, hereinafter. Then, the upper electrode 270 is formed on the dielectric layer 260, thus completing the capacitor of the present invention.

Here, since the first diffusion barrier layer pattern 240 makes no contact with the amorphous dielectric layer, oxidation of the first diffusion barrier layer pattern 240 is prevented during the heat-treatment. When the dielectric layer 260 is formed in in-situ, oxidation of the diffusion first barrier layer pattern 240 is prevented because the first diffusion barrier layer pattern 240 is not exposed to an oxygen atmosphere.

Furthermore, reaction between oxygen introduced through the conductive layer pattern 250 and the first diffusion barrier layer pattern 240 can be prevented by forming the second diffusion barrier layer pattern 247.

As described above, in the present invention, reduction of the capacitance of the capacitor due to oxidation of a portion of the lower electrode can be prevented by preventing oxidation of the diffusion barrier layer pattern 140 or the first diffusion barrier layer pattern 240.

Claims

1. A method of manufacturing a capacitor for a semiconductor device, comprising the steps of:

   (a) forming a first interlayer insulating layer having a first contact hole on a semiconductor substrate;
   (b) forming a contact plug to fill said first contact hole;
   (c) forming a diffusion barrier layer pattern on said contact plug;
   (d) forming a second interlayer insulating layer pattern having a second contact hole which exposes said diffusion barrier layer pattern on the resultant including the diffusion barrier layer pattern;
   (e) forming a conductive layer pattern to make contact with said diffusion barrier layer pattern through said second contact hole to complete a lower electrode including said contact plug, said diffusion barrier layer pattern, and a conductive layer pattern; and
   (f) sequentially forming a dielectric layer and an upper electrode on said conductive layer pattern.

2. A method according to claim 1, wherein the diffusion barrier layer pattern is formed of one selected from a group consistng of Ta, Co, TiN, (Ti, Al)N, (Ti, Si) N, TaN, (Ta, Si)N, TiSix, TaSix, and CoSix.

3. A method according to claim 1 or 2, wherein the conductive layer pattern is formed of one selected from a group consisting of platinum (Pt), iridium (Ir), ruthenium (Ru), iridium dioxide (IrO_2), and ruthenium dioxide (RUO_2).

4. A method according to any preceding claim, wherein the contact plug, said diffusion barrier layer pattern, and said conductive layer pattern are formed of impurity-doped plysilicon, titanium nitride (TiN), and platinum (Pt), respectively.

5. A method of manufacturing a capacitor for a semiconductor device, comprising the steps of:

(a) forming a first interlayer insulating layer pattern having a first contact hole on a semiconductor substrate;
(b) forming a contact plug to fill the first contact hole;
(c) forming a first diffusion barrier layer pattern on the contact plug;
(d) forming a second interlayer insulating layer pattern having a second contact hole which exposes the first diffusion barrier layer pattern on the resultant including said first diffusion barrier layer pattern;
(e) forming a second diffusion barrier layer pattern to rill the second contact hole;
(f) forming a conductive layer pattern on the second diffusion barrier layer pattern to complete a lower electrode including the contact plug, said first diffusion barrier layer pattern, said second diffusion barrier layer pattern, and the conductive layer pattern; and
(g) sequentially forming a dielectric layer and an upper electrode on the conductive layer pattern.

6. A method according to claim 5, wherein the first diffusion barrier layer pattern is formed of one selected from a group consistng of Ta, Co, TiN; (Ti, Al)N, (Ti, Si)N, TaN, (Ta, Si)N, TiSix, TaSix, and CoSix.

7. A method according to claim 5 or 6, wherein the second diffusion barrier layer pattern is formed of one selected from a group consisting of Ir, Ru, IrO_2, and RUO_2.

8. A method according to any one of claims 5 to 7, wherein the conductive layer pattern is formed of Pt.

9. A method according to any one of claims 5 to 8, wherein the second diffusion barrier layer is formed to have a double-layer structure where Ir and IrO_2 are sequentially stacked, and the conductive layer pattern is formed of Pt.

10. A method according to any preceding claim, wherein said contact plug is formed of one selected from a group consisting of impurity-doped polysilicon, tungsten (W), tungsten nitride (WN), and tungsten silicide (WSix).

FIG. 1 (PRIOR ART)

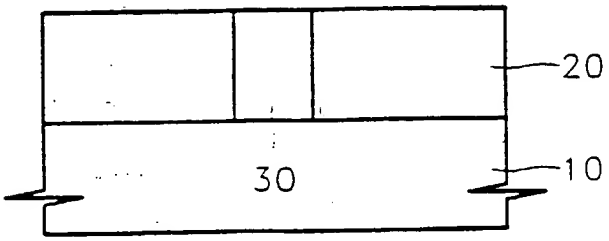

FIG. 2 (PRIOR ART)

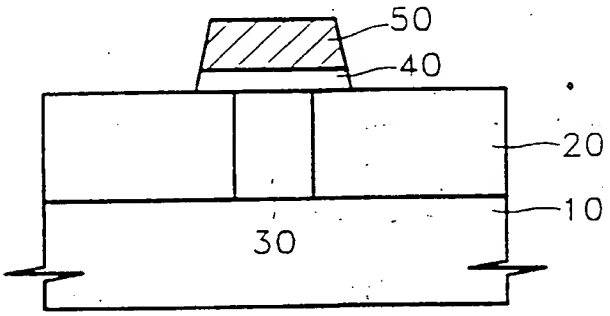

FIG. 3 (PRIOR ART)

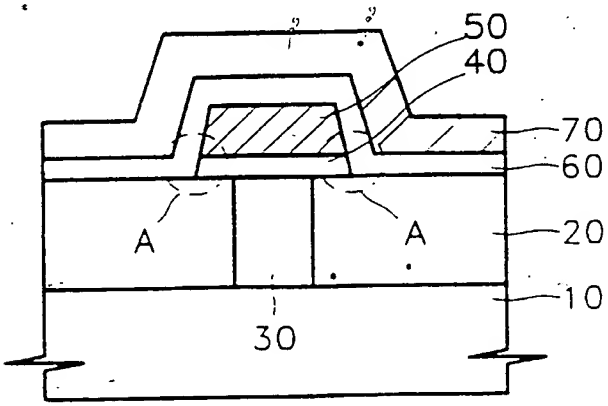

FIG. 4

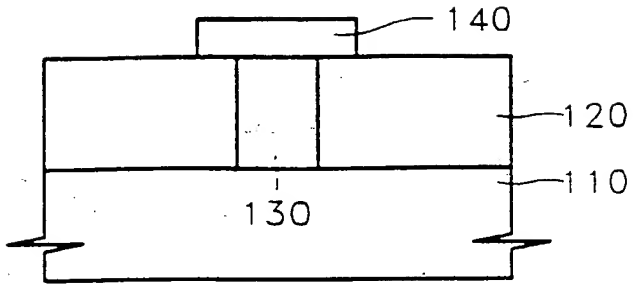

FIG. 5

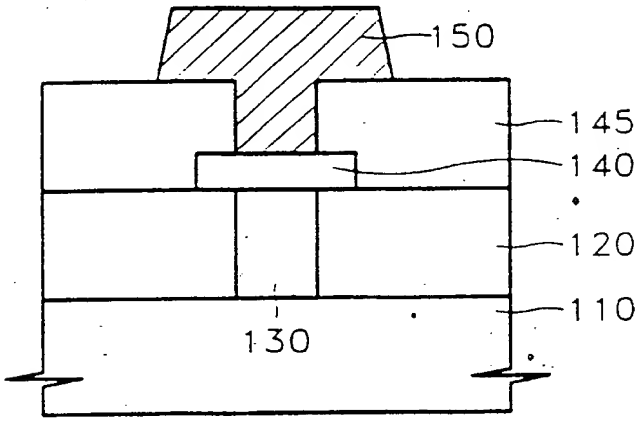

FIG. 6

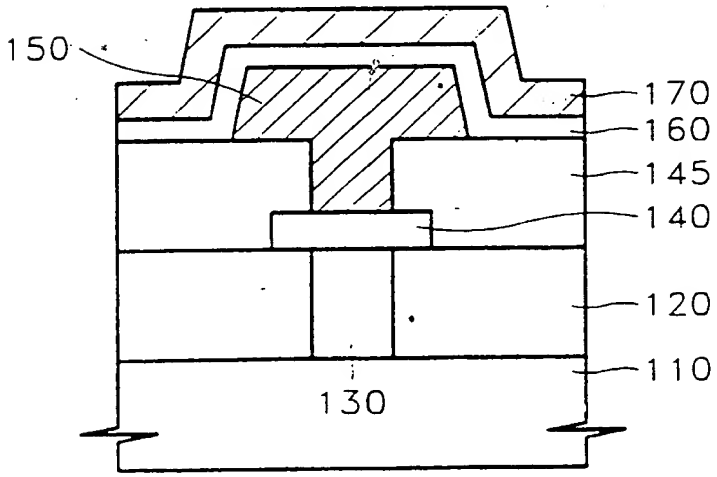

FIG. 7

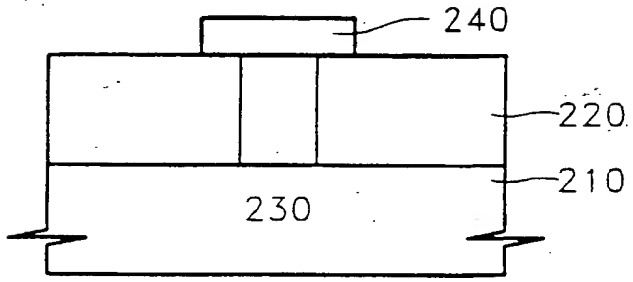

FIG. 8

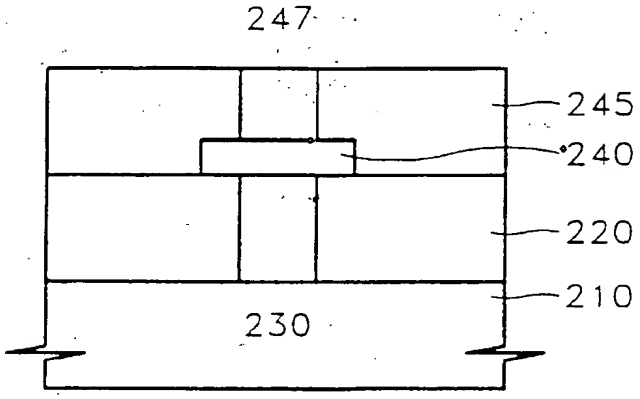

FIG. 9